EGC220
Class Notes
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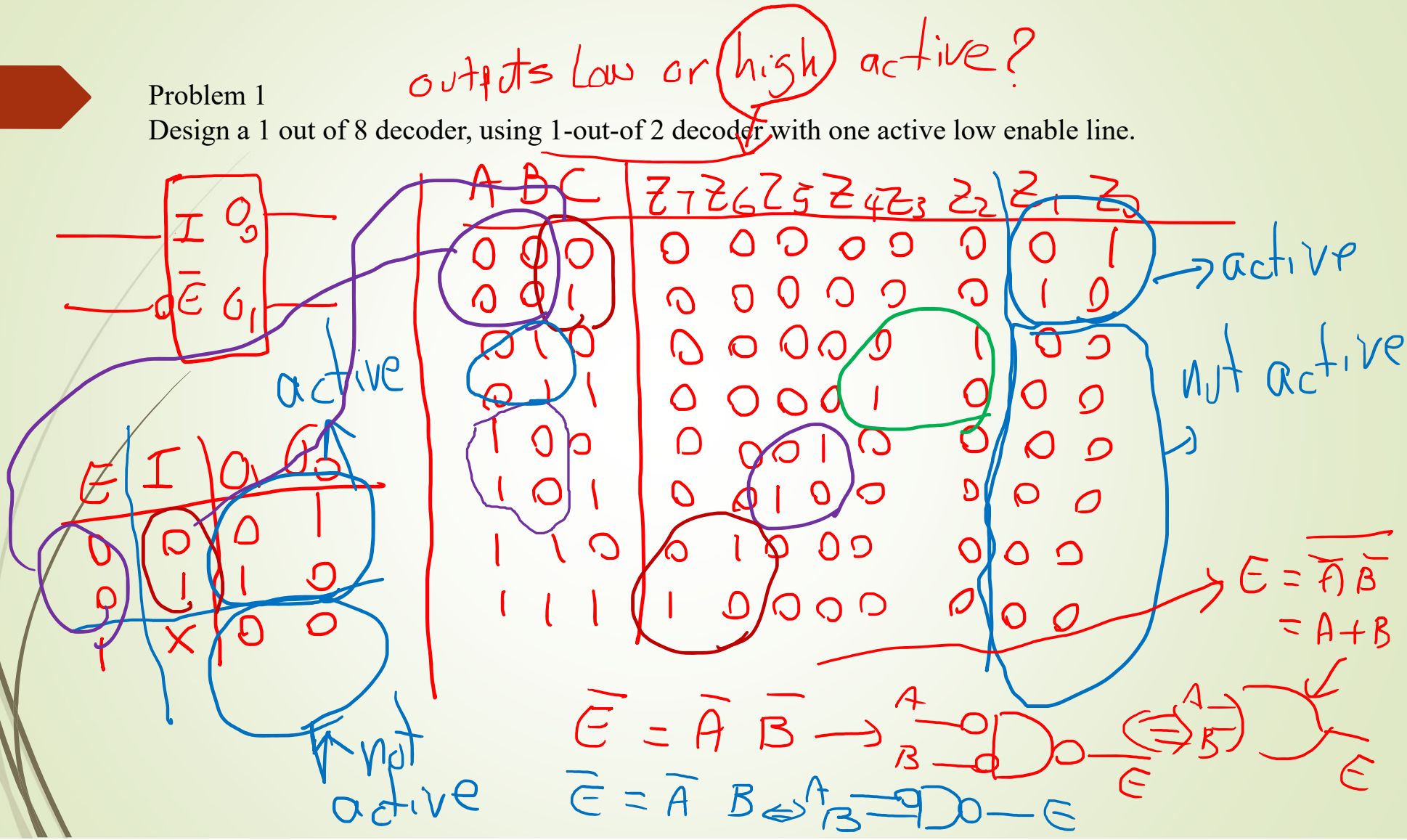
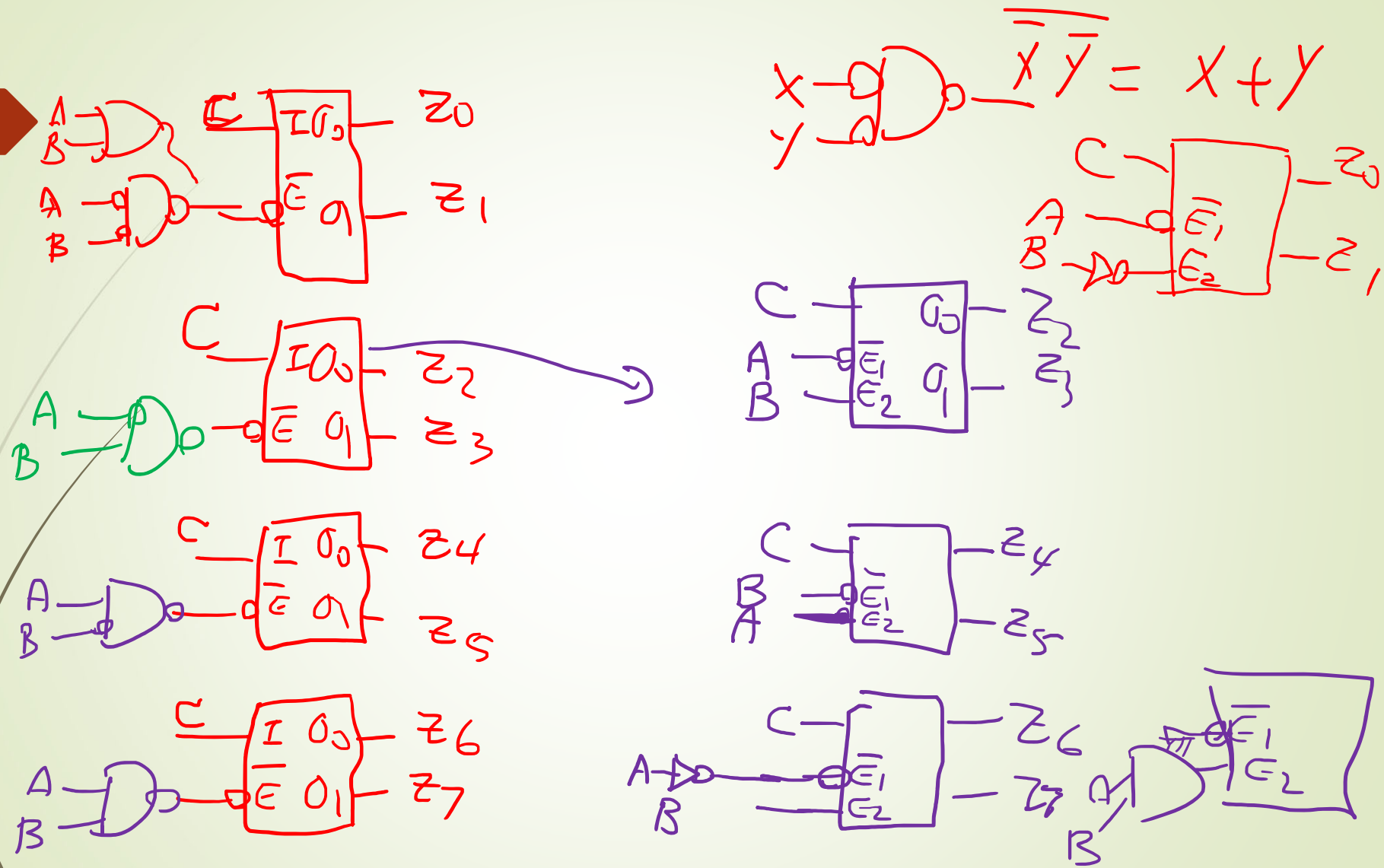
Problem 1

Design a 1 out of 8 decoder, using 1-out-of 2 decoder with one active low enable line.

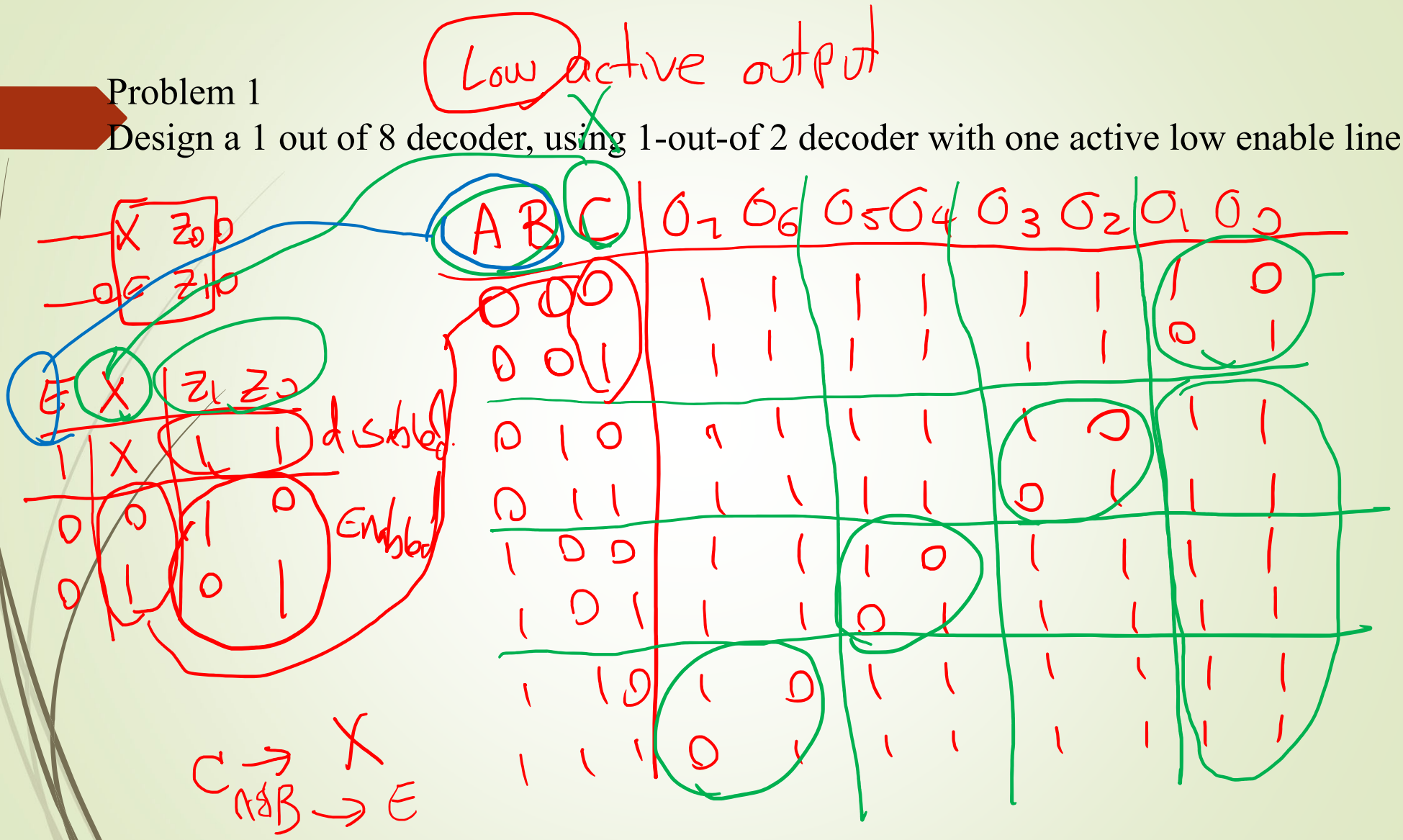


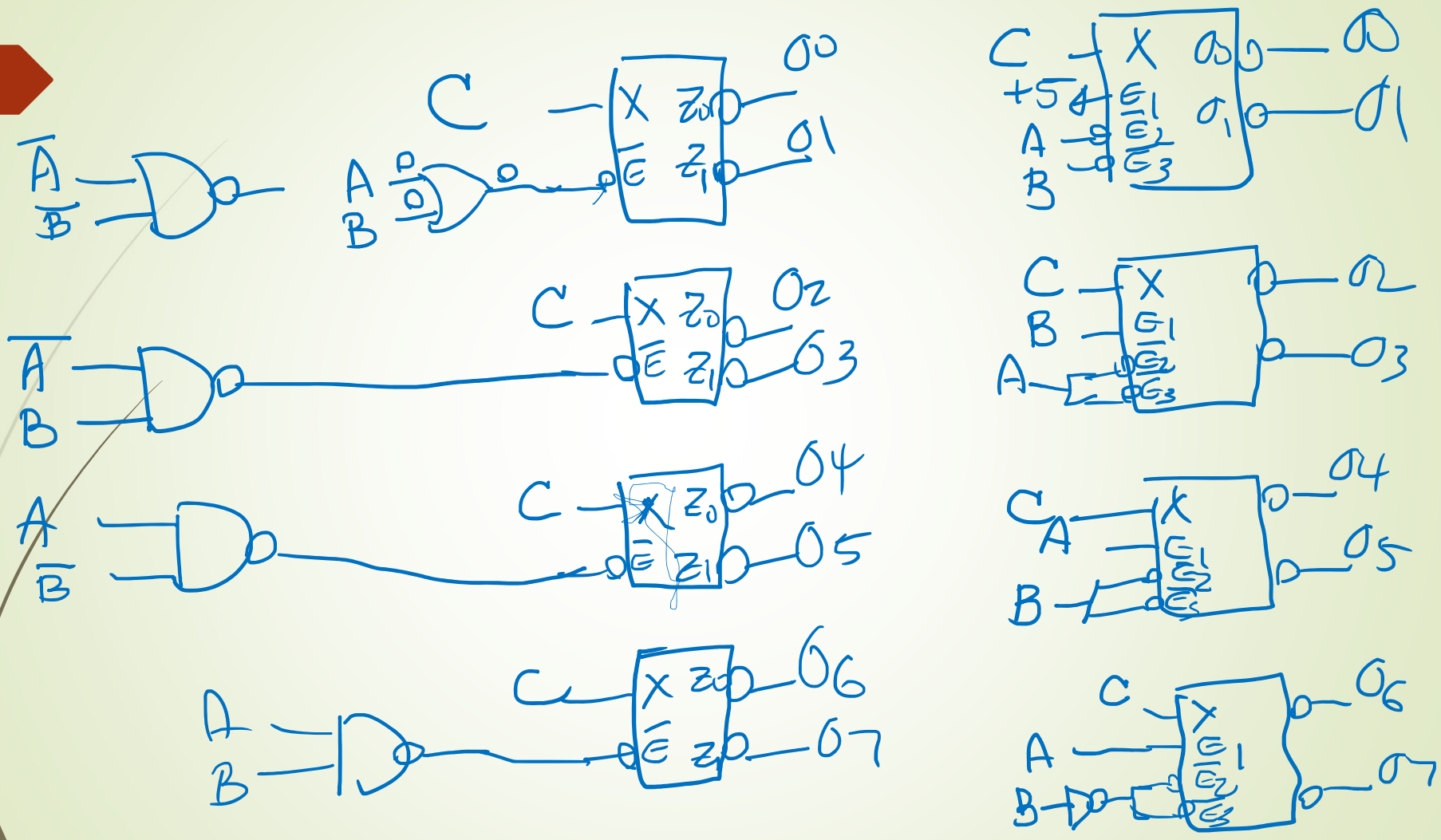


$\overline{\overline{X}\,\overline{Y}} = X + Y$
A
B
C
I
O_0
$\overline{E}$
O_1
Z_0
Z_1
Z_2
Z_3
Z_4
Z_5
Z_6
Z_7
X
Y
$\overline{E}_1$
E_2

Problem 1

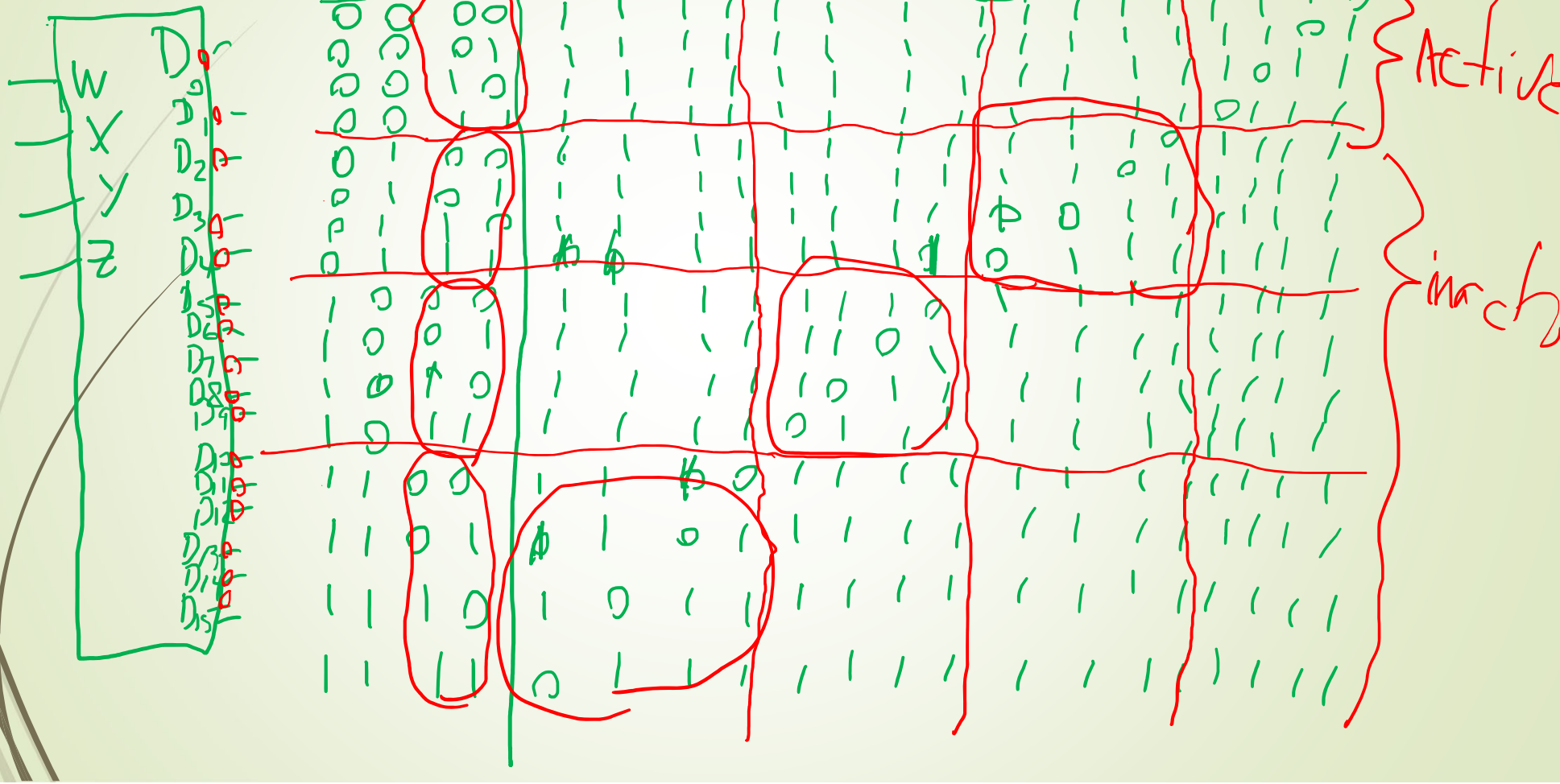
Design a 1 out of 8 decoder, using 1-out-of 2 decoder with one active low enable line.

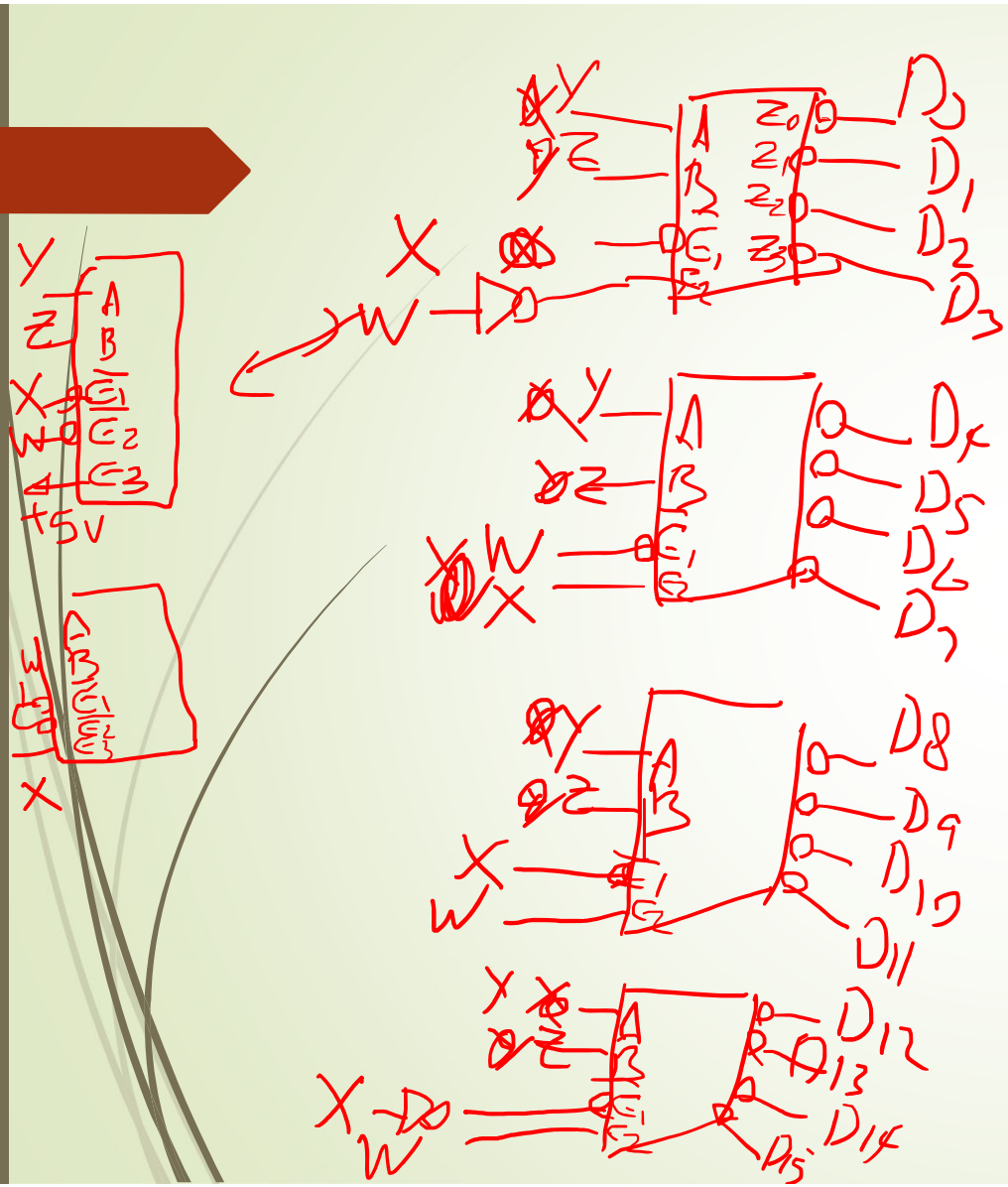



A
B
C
X
Z0
E
Z1
O0
O1
O2
O3
O4
O5
O6
O7
+5
G1
G2
G3

Problem 3

Using the decoder in Problem 3, design a 1 out of 16 decoder with active low outputs.





E_1	E_2	A B	Z_3	Z_2	Z_1	Z_0	
1	X	X X	1	1	1	1	In active
X	0	X X	1	1	1	1	
0	1	0 0	1	1	1	0	
0	1	0 1	1	1	0	1	
0	1	1 0	1	0	1	1	
0	1	1 1	0	1	1	1	

W & X

X 2

Problem 4

Write a Verilog code for the decoder in Problem 2: 1-out of 4 decoder active low outputs and two enable lines, one active low and one active high.

```
module decoder-1-out-4 (EN, E, A, B, O0, O1, O2, O3);
input EN, E, A, B;
output O0, O1, O2, O3;
Assign ~O0 = ~EN & E & ~A & ~B;
Assign ~O1 = ~EN & E & ~A & B;
Assign ~O2 = ~EN & E & A & ~B;
Assign ~O3 = ~EN & E & A & B;
endmodule
```

$\overline{O_0} = \overline{EN} \cdot E \cdot \overline{A} \cdot \overline{B}$

```
// 2-to-4-Line Decoder with Enable: Dataflow Verilog Desc.          //  1
// (See Example 3-16 for logic diagram)                             //  2
module decoder_2_to_4_df_v(EN, A0, A1, D0, D1, D2, D3);             //  3
   input EN, A0, A1;                                                //  4
   output D0, D1, D2, D3;                                           //  5
                                                                    //  6
   assign D0 = EN & ~A1 & ~A0;                                      //  7
   assign D1 = EN & ~A1 & A0;                                       //  8
   assign D2 = EN & A1 & ~A0;                                       //  9
   assign D3 = EN & A1 & A0;                                        // 10
                                                                    // 11
endmodule                                                           // 12
```

$D_0 = EN \cdot \overline{A_1} \cdot \overline{A_0}$

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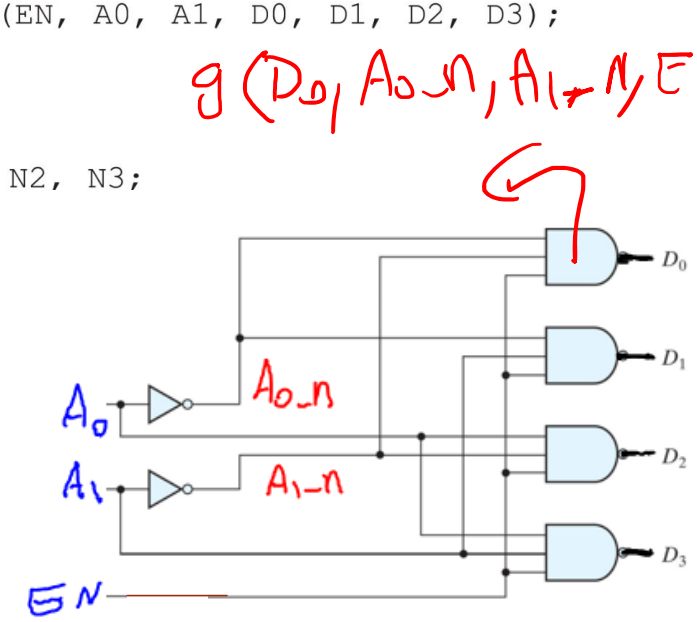
Structural Verilog Description of 2–to–4-Line Decoder

```
// 2-to-4-Line Decoder with Enable: Structural Verilog Desc.          //  1
// (See Figure 3-16 for logic diagram)                                //  2
module decoder_2_to_4_st_v (EN, A0, A1, D0, D1, D2, D3);              //  3
   input EN, A0, A1;                                                  //  4
   output D0, D1, D2, D3;                                             //  5
                                                                      //  6
   wire A0_n, A1_n, N0, N1, N2, N3;                                   //  7
   not                                                                //  8
      g0(A0_n, A0),                                                   //  9
      g1(A1_n, A1);                                                   // 10
   and                                                                // 11
      g3(N0, A0_n, A1_n),                                             // 12
      g4(N1, A0, A1_n),                                               // 13
      g5(N2, A0_n, A1),                                               // 14
      g6(N3, A0, A1),                                                 // 15
      g7(D0, N0, EN),                                                 // 16
      g8(D1, N1, EN),                                                 // 17
      g9(D2, N2, EN),                                                 // 18
      g10(D3, N3, EN);                                                // 19
endmodule                                                             // 20
```



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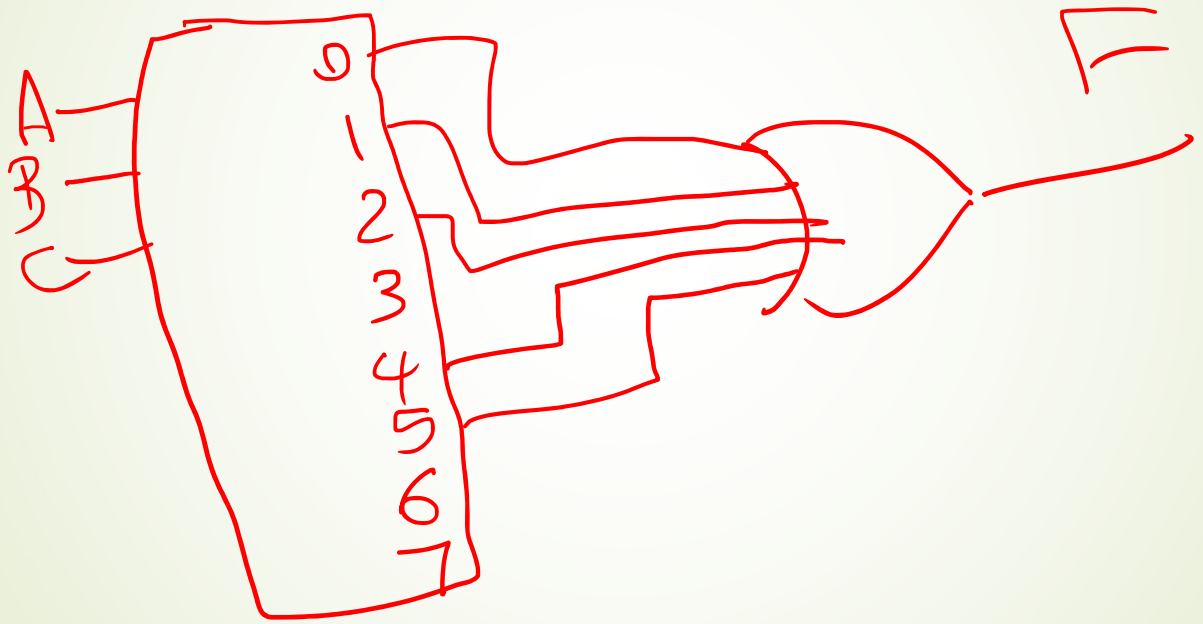
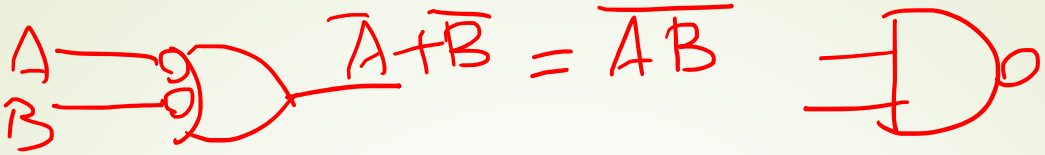
Problem 2

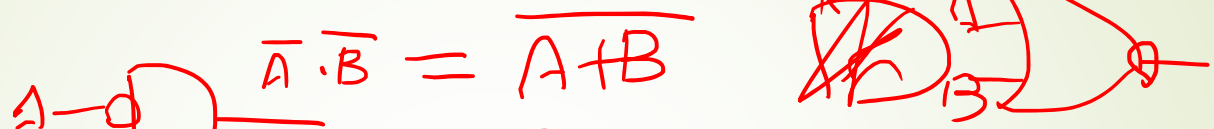
Implement the following Boolean expression using a decoder and an OR gate – You may choose a decoder with active high or active low outputs.

$F(A,B,C,D) = \sum m\,(0, 1, 2, 4, 5) + d(3, 7)$



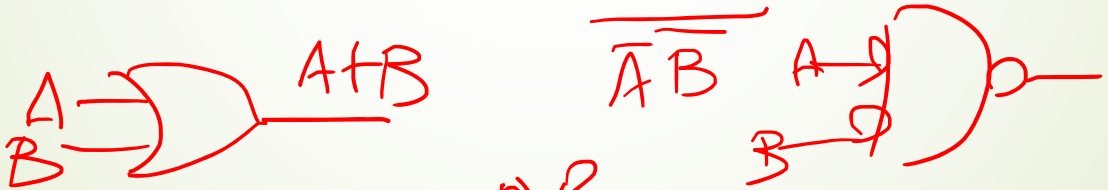
NAND



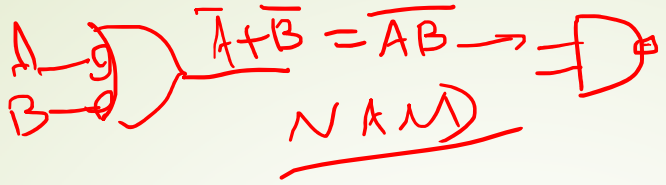


NOR

AND



OR



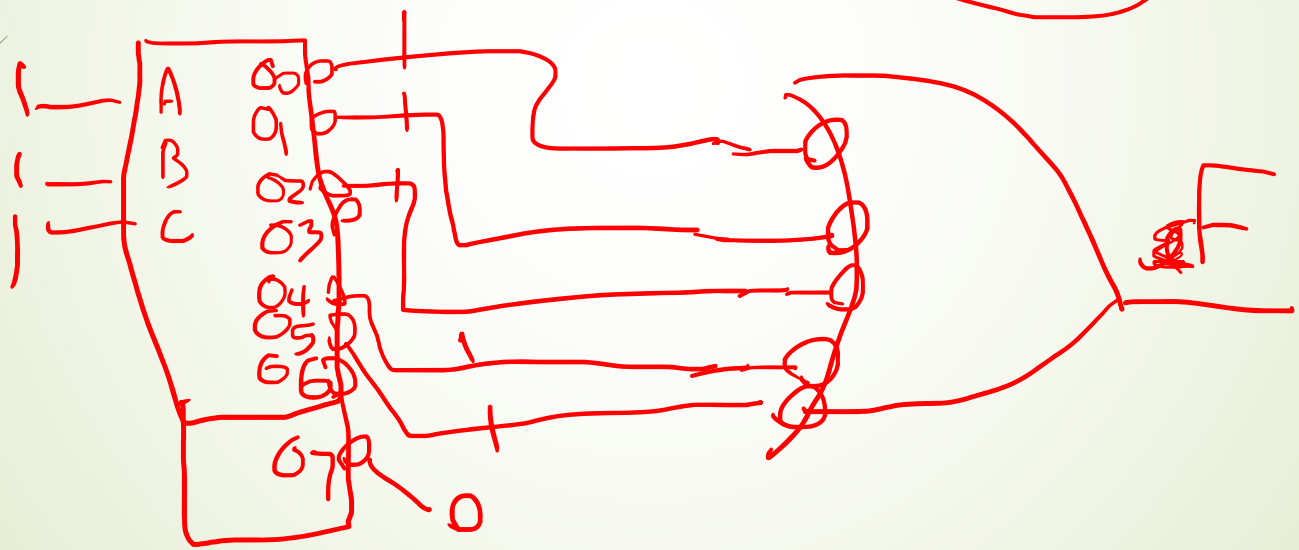
Problem 2

Implement the following Boolean expression using a decoder and an OR gate – You may choose a decoder with active high or active low outputs.

NAND

$F(A,B,C) = \sum m(3,7) + d(6)$

$F(A,B,C,D) = \sum m(0, 1, 2, 4, 5) + d(6)$

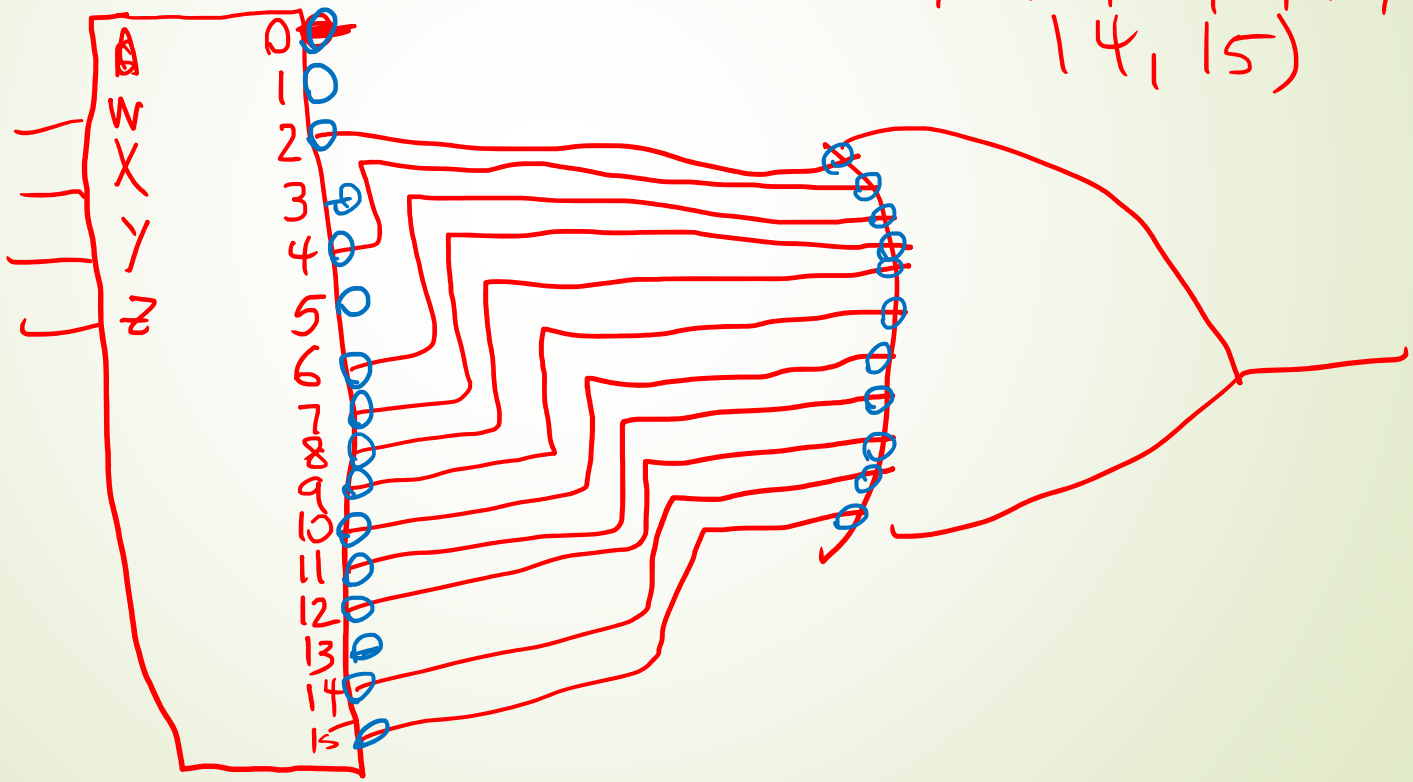


Problem 3

Implement the following Boolean expression using a decoder and an OR gate – You may choose a decoder with active high or active low outputs.

NAND

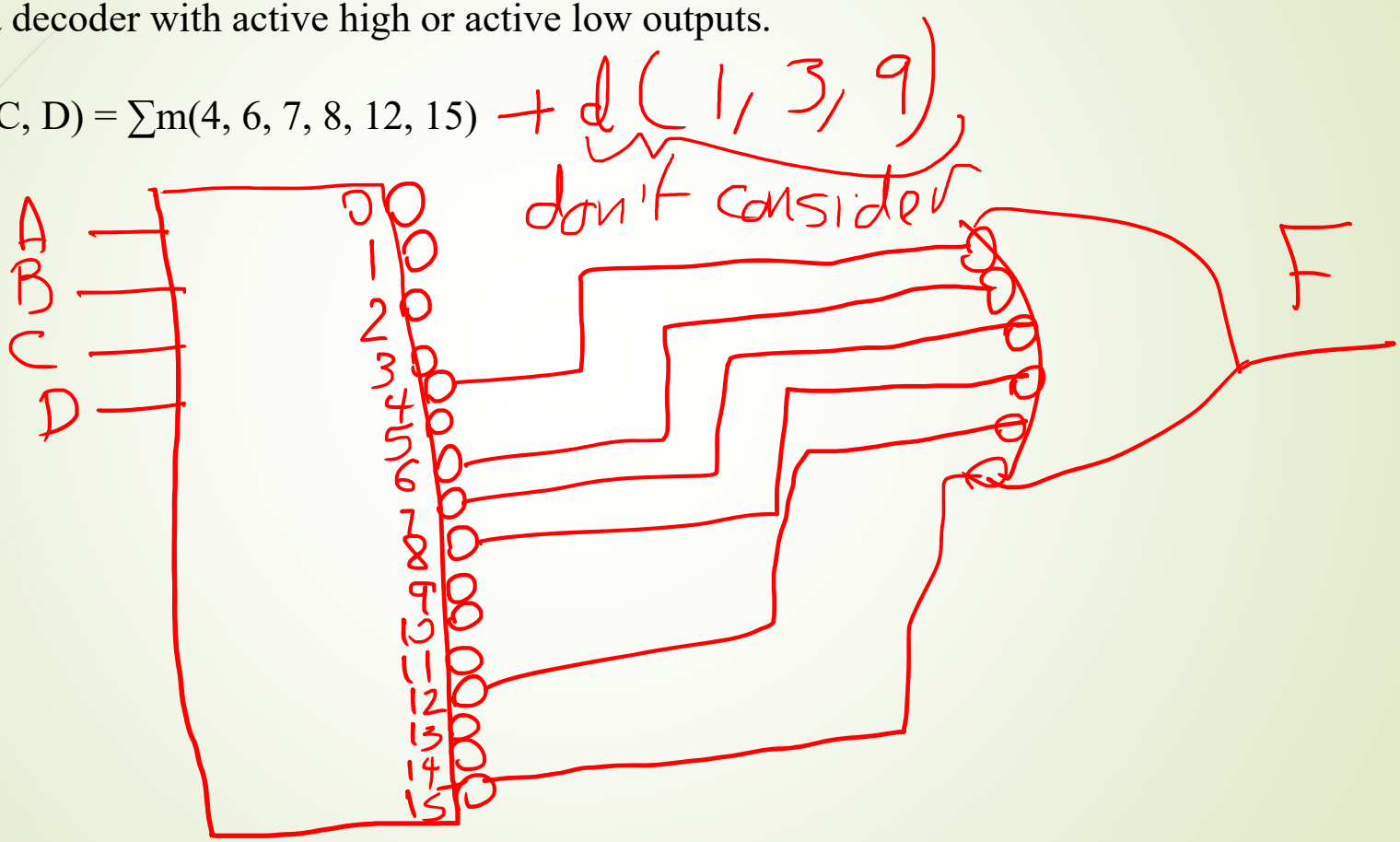
$f(w, x, y, z) = \Pi M(0, 1, 3, 5, 13)$ $= \Sigma m(2, 4, 6, 7, 8, 9, 10, 11, 12, 14, 15)$



Problem 4

Implement the following Boolean expression using a decoder and a NAND gate – You may choose a decoder with active high or active low outputs.

$F(A, B, C, D) = \sum m(4, 6, 7, 8, 12, 15) + d(1, 3, 9)$

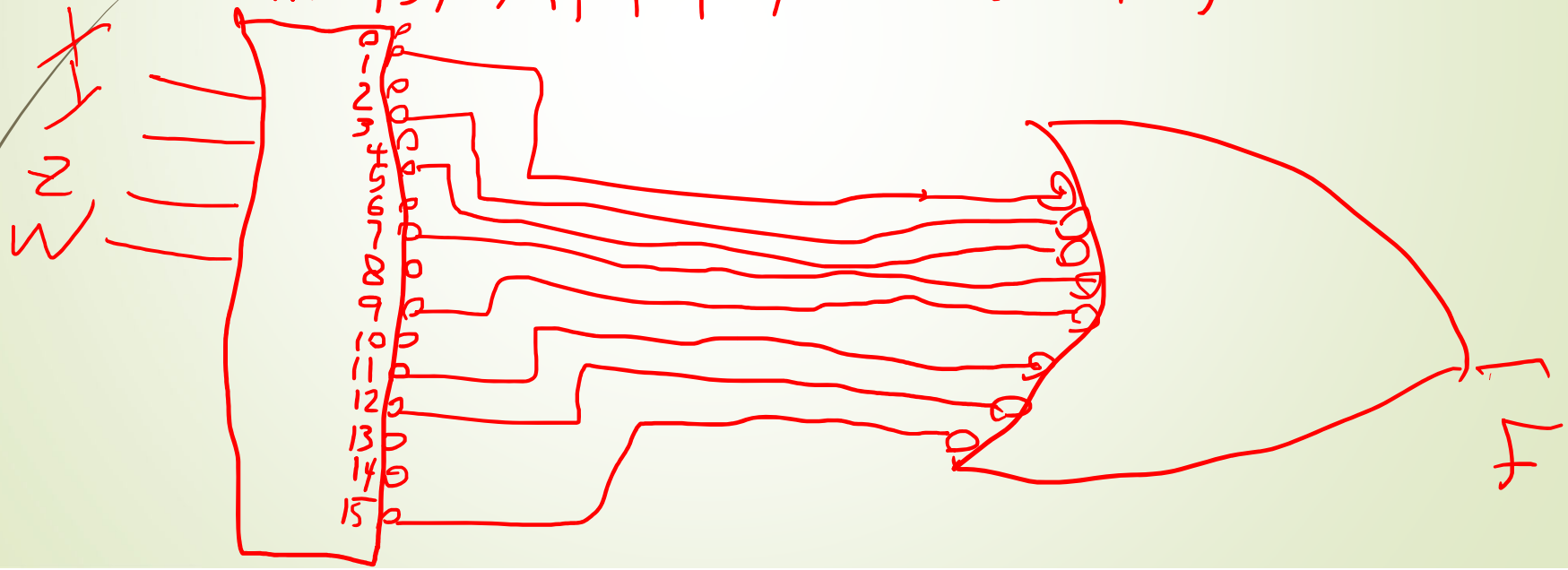


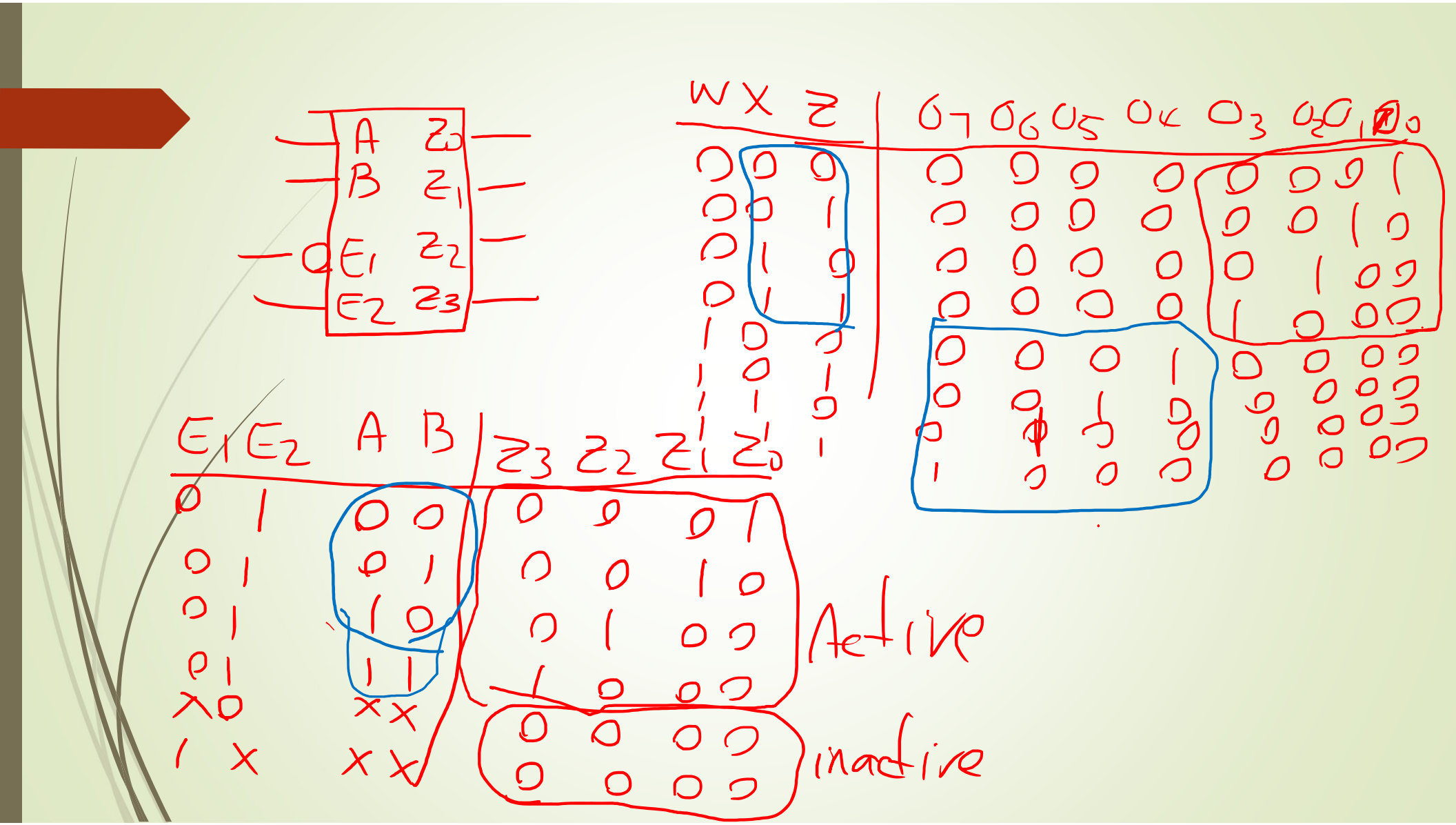
Problem 5

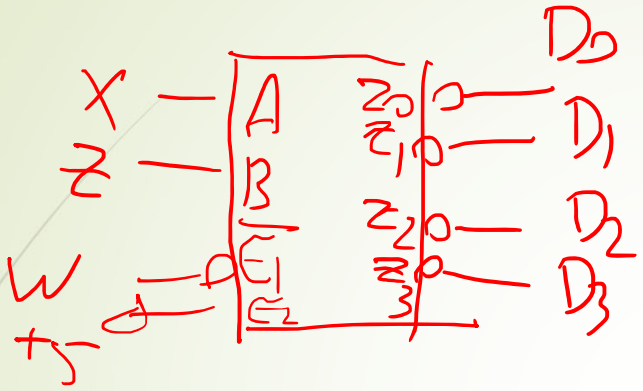
Implement the following Boolean expression using a decoder and a NAND gate – You may choose a decoder with active high or active low outputs.

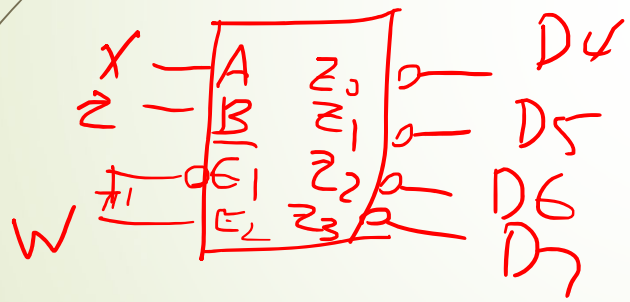
$F(X, Y, Z, W) = \prod M(0, 6, 8, 13, 14) + d(2, 4, 10)$

$F = \Sigma m(1, 3, 5, 7, 9, 11, 12, 15) + d(2, 4, 10)$




A
B
E1
E2
Z0
Z1
Z2
Z3
W X Z
O7 O6 O5 O4 O3 O2 O1 O0
E1 E2 A B
Z3 Z2 Z1 Z0
Active
inactive


X
Z
W
+5
A
B
E1
E2
Z0
Z1
Z2
Z3
D0
D1
D2
D3


X
Z
W
A
B
E1
E2
Z0
Z1
Z2
Z3
D4
D5
D6
D7